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EXAMINER

TRAN, DENISE

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 04/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/466,180	CAMERON ET AL.
	Examiner Denise Tran	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 December 1999.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4, 8-12 and 15-20 is/are rejected.

7) Claim(s) 5-7, 13 and 14 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.

2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) Other: _____

DETAILED ACTION

1. Claims 1-20 are pending in the application.
2. The disclosure is objected to because of the following informalities: the application should be claimed benefits under 35 U.S.C. 119e instead of 35 U.S.C. 120 as recited on page 1, line 6 of the specification.

Appropriate correction is required.

3. Claims 5-7, and 13-14, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach the use of wherein each of the translation and protection table entries, comprises protection attributes which control read and write access to a given memory region of the host memory; the translation cacheable flag which specifies whether the host fabric adapter flushes a corresponding translation and protection table entry stored in the internal cache; a physical page address field which addresses a physical page frame of data entry; and a memory protection tag which specifies whether the host fabric adapter has permission to access the host memory.

Art Unit: 2186

4. Claims 19-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. The prior art of record does not teach the use of wherein each of the translation and protection table entries, comprises protection attributes which control read and write access to a given memory region of a host memory; the translation cacheable flag which specifies whether the apparatus flushes a corresponding translation and protection table entry stored in the internal cache; a physical page address field which addresses a physical page frame of data entry; and a memory protection tag which specifies whether the apparatus has permission to access the host memory.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 16, it is unclear where the preamble and body of the claim are. It is confusing because there are no means for flushing and storing the table entry.

Art Unit: 2186

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), in view of Watkins, U.S. Patent No. 5,937,436.

As per claim 16, Horstmann shows the invention substantially as claimed, an apparatus that stores translation table entries for virtual to physical address translations (e.g., col. 3, lines 54-60), and which flushes individual translation table entry stored in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35).

Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the translation table entries of Horstmann because it would

Art Unit: 2186

provide protection of read only memory pages, thereby increasing data security from unwanted writing.

As per claim 17, Horstmann shows the apparatus comprises an internal cache for storing the translation table entries (e.g., col. 3, lines 54-60). Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the translation table entries of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), in view of Watkins, U.S. Patent No. 5,937,436; and further in view of Futral, U.S. Patent No. 6,112,263.

As per claim 18, Horstmann shows wherein each of the translation table entries represents translation of a single page of a memory (e.g., col. 1, lines 56-60; col. 2, lines 8-14; col. 3, lines 65-67). Horstmann does not explicitly show the use of protection in the translation table entries and a host memory. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection

Art Unit: 2186

translation table entries and a workstation (e.g. figure 2A, element 200) comprising a main memory (e.g. figure 2A, element 220), a workstation fabric adapter (e.g. figure 2A, element 260k). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Watkins into the system of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing. Watkins and Horstmann do not explicitly show the use of a host memory. Futral shows the use of a host comprising a host memory (e.g. col. 1, lines 37-45; col. 7, lines 47- 55; figure 2a, el. 212 comprising el. 230). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer having a memory storing its data in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28).

10. Claims 1-4, 8-12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (5,937,436), in view of Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), and further in view of Futral, U.S. Patent No. 6,112, 263.

Art Unit: 2186

As per claim 1, Watkins shows of the invention substantially as claimed, a workstation (e.g., fig.2A, el. 200, col. 3, line 34) coupled to a switched fabric (e.g., fig.3, an ATM Switch and network; col. 3, lines 14-18), comprising:

a processor (e.g. figure 2A, element 210);

a main memory coupled to the processor (e.g. figure 2A, element 220);

and

a workstation fabric adapter (e.g. figure 2A, element 260K) coupled to the processor and provided to interface with the switched fabric (e.g., fig.3, an ATM Switch and network; col. 3, lines 14-18), which caches (i.e., frequently used data values being duplicated for quick access) selected translation and protection table (TPT) entries from the memory for a data transaction (e.g., figure 4, element 450 and col. 2, lines 14-18; col. 1, lines 54-65; col. 6, lines 5-14; col. 6, lines 49-65 and col. 7, lines 60-65), and flushes individual cached translation and protection table (TPT) entry (e.g. col. 2, lines 19-22, col. 9, lines 13-15 and 65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed

Art Unit: 2186

by limiting number of reloading currently used data, reduce chip area for fabrication, support efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212) and fabric-attached I/O controllers (e.g. fig. 2a, el. 218; col. 6, lines 28-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching the host of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching fabric-attached I/O controllers of Futral with Watkins and Horstmann because it would provide circuits for controlling I/O devices and freeing the host's time for other work; and increase system scalability and availability, thereby allowing more users to be supported as taught by Futral col. 1, lines 32-45.

As per claim 2, Watkins shows the use of the adapter comprises an internal cache memory (i.e., a memory in which frequently used data values

Art Unit: 2186

being duplicated for quick access) for storing a set of translation and protection table entries from the memory (e.g., figure 4, element 450 and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

As per claim 3, Watkins shows the use of each of the selected translation and protection table entries as a page of the main memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

Art Unit: 2186

As per claim 4, Watkins shows the use of the adapter is provided to perform virtual to physical address translations and validate access to the memory using the selected translation and protection table entries (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

As per claim 8, Watkins shows the use of the adapter flushing of a table entry by software (e.g., col.7, lines 26-27 and col.10, lines 26-28). Watkins does not specifically show the use of an operating system including driver software to set the status of the translation cacheable flag per translation and protection table entry for enabling flushing individual cached translation and protection table entry from the internal cache. Horstmann shows an operating system (e.g., col. 1, lines 16-19); and software of the operating system setting the status of the translation cacheable flag per translation and protection table entry for enabling flushing individual cached translation and protection table entry from the internal

Art Unit: 2186

cache (e.g., col. 11, lines 25-35 and col. 10, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of the operating system of Horstmann into the system of Watkins because it would provide efficiently supporting overall control of many concurrent processes running within the system, supervising the allocation and usage of system hardware resources such as setting the status of the translation cacheable flag per translation and protection table entry for enabling flushing individual cached translation and protection table entry from the internal cache as taught by Horstmann, col.1, lines 41-55 and col. 11, lines 25-35; thereby it would increase translation speed by limiting number of reloading currently used data, reduce chip area for fabrication, supports efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

Watkins, Horstmann, and Futral do not specifically show the use of a driver to run an adapter. "Official Notice" is taken that both the concept and the advantages of having a drive is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver for the adapter to the combined system of Watkins, Horstmann, and Futral because it would allow the operating system to

Art Unit: 2186

communicate with the internal components to update, complete transactions with and control a variety of I/O interfaces, such as network interface.

As per claim 9, Watkins shows a network (e.g., ATM network col. 3, lines 10-20), comprising:

a switched fabric (e.g. figure 3, an ATM switch and network and col. 3, lines 10-20); and

a workstation (e.g. figure 2A, element 200) comprising a main memory (e.g. figure 2A, element 220), a workstation fabric adapter (e.g. figure 2A, element 260k) which caches (i.e., frequently used data values being duplicated for quick access) selected translation and protection table (TPT) entries from the main memory (e.g., figure 4, element 450 and col.1, lines 54-65; col. 2, lines 14-22; col. 6, lines 5-10; col. 6, lines 49-65 and col. 7, lines 60-65), and which flushes individual cached translation and protection table (TPT) entry (e.g. col. 2, lines 19-22, col. 6, lines 9-13 and col. 9, lines 9-65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag and an operating system. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35) and the use of operating system (e.g., col. 1, lines 17-19 and col. 1, lines 49-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching the corresponding translation cacheable flag of

Art Unit: 2186

Horstmann into the system of Watkins because it would increase translation speed from limiting number of reloading currently used data, reduce chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49. Also, It would have been obvious to one of ordinary skill in the art at the time the invention was made to have apply the teaching operating system of Horstmann into the system of Watkins because it would provide the overall control of many concurrent processes running within the system, supervising the allocation and usage of system hardware resources, scheduling operations and preventing interference between different programs as teaching in Horstmann col.1, lines 39-55.

Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 1, el. 212), fabric-attached I/O controllers (e.g. fig. 1, el. 218; col. 6, lines 28-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching the host of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link and provide many concurrent processes running within the system in controlled and secure manner as teaching by Futral col. 2, lines 49-51 and col. 2, lines 25-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching the fabric-attached

Art Unit: 2186

I/O controllers of Futral with Watkins and Horstmann because it would provide circuits for controlling I/O devices and freeing the host's time for other work; and increase system scalability, availability, thereby allow more users to be supported as taught by Futral col. 1, lines 32-45.

As per claim 10, Watkins shows the use of the adapter comprises an internal cache memory (i.e., a memory in which frequently used data values being duplicated for quick access) for storing a set of translation and protection table entries from the memory (e.g., figure 4, element 450 and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

As per claim 11, Watkins shows the use of each of the selected translation and protection table entries as a page of the main memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1,

Art Unit: 2186

lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

As per claim 12, Watkins shows the use of the adapter is provided to perform virtual to physical address translations and validate access to the memory using the selected translation and protection table entries (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col. 1, lines 64-68). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link, provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

As per claim 15, Watkins shows wherein the adapter flushing a cached translation and protection table entry from the internal cache (e.g. col. 2, lines 19-22, col. 6, lines 9-13 and col. 9, lines 9-65). Watkins does not explicitly show

Art Unit: 2186

flushing a designate cache when the translation cacheable flag of the designated cache table entry indicated a first logic state and maintained the designated table entry for future re-used when the flag of the designated table entry indicated a second logic opposite of the first logic state. Horstmann shows the use of flushing a designate cache when the translation cacheable flag (e.g., valid bit) of the designated cache table entry indicated a first logic state and maintain the designated table entry for future re-used when the flag of the designated table entry indicated a second logic opposite of the first logic state (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed from limiting a number of reloading currently used data, reduced chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses. Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral shows the use of a host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled

Art Unit: 2186

and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a) Davidson, Jr. et al. (5550957) shows the use of multiple hosts connecting to a network printer;
- b) Gaytan et al. (5633870) shows the use of the internal structure of an ATM network;

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday, and an alternate Wed. from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7467-239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Art Unit: 2186

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Deupree

D.T.
April 5, 2002